



PTO/SB/08A (08-03)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known

Application Number	10/728,570
Filing Date	December 5, 2003
First Named Inventor	M. Riedel
Art Unit	2818 2825
Examiner Name	Not yet assigned LIN, SUN J.
Attorney Docket Number	18021-6226

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
JFA	A	US- 6,105,139	08/15/2000	Dey et al.	
JFA	B	US- 6,430,726	08/06/2002	Nakamura	
JFA	C	US- 6,591,231	07/08/2003	Kurshan et al.	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	<i>James P. Smith</i>	Date Considered	3-3-06
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Application Number	10/728,570
Filing Date	December 5, 2003
First Named Inventor	M. Riedel
Art Unit	2819 2825
Examiner Name	Not yet assigned LIN, SUN J.
Attorney Docket Number	18021-6226

Sheet


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of

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JSR	D	International Search Report for International PCT Application PCT/US03/38622 dated May 4, 2004.	
	E	Robert Allen Short, "A Theory of Relations Between Sequential and Combinational Realizations of Switching Functions", February 1961, pp. 1-115.	
	F	William H. Kautz, "The Necessity of Closed Circuit Loops in Minimal Combinational Circuits", IEEE Transactions on Computers, February 1970, pp. 162-164.	
	G	David A. Huffman, "Combinational Circuits with Feedback", pp. 27-55.	
	H	Ronald L. Rivest, "The Necessity of Feedback in Minimal Monotone Combinational Circuits", IEEE Transactions on Computers, June 1977, pp. 606-607.	
	I	Leon Stok, "False Loops through Resource Sharing", IEEE, 1992, pp. 345-348.	
	J	Sharad Malik, "Analysis of Cyclic Combinational Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 7, July 1994, pp. 950-95	
	K	Anand Raghunathan et al., "Test Generation for Cyclic Combinational Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 11,	
	L	Arvind Srinivasan et al., "Practical Analysis of Cyclic Combinational Circuits", IEEE Custom Integrated Circuits Conference, 1996, pp. 381-384.	
JSR	M	Thomas Robert Shiple et al., "Formal Analysis of Synchronous Circuits", pp. 1-202.	

Examiner Signature		Date Considered	3-3-06
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		Application Number	10/728,570
		Filing Date	December 5, 2003
		First Named Inventor	M. Riedel
		Art Unit	2819 2825
Examiner Name	Not yet assigned LIN, SUN J.		
Attorney Docket Number	18021-6226		
Sheet	3	of	3

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JSL	N	Thomas R. Shiple et al., "Analysis of Combinational Cycles in Sequential Circuits", IEEE International Symposium on Circuits and Systems, Vol. 4, 1996, pp. 592-595.	
	O	Thomas R. Shiple et al., "Constructive Analysis of Cyclic Circuits", Paris, March 1996, pp. 1-6.	
	P	Robert de Simone, "Note: A Small Hardware Bus Arbiter Specification Leading Naturally to Correct Cyclec Description", March 1996, pp. 1-8.	
	Q	Amar Bouali et al., "Verifying Synchronous Reactive Systems Programmed in ESTEREL", pp. 1-4.	
	R	Stephen A. Edwards, "Making Cyclic Circuits Acyclic", pp. 159-162.	
	S	R. K. Brayton et al., "Multilevel Log Synthesis", Proceedings of the IEEE, Vol. 78, No. 2, February 1990, pp. 264-300.	
JSL	T	Randal E. Bryant, "Boolean Analysis of MOS Circuits", IEEE Trans. Computer-Aided Design, February 1987, pp. 1-32.	

Examiner Signature	<i>James Sun Jin</i>	Date Considered	3-3-06
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		Application Number	10/728,570		
		Filing Date	12/05/2003		
		First Named Inventor	M. Riedel		
		Art Unit	2819 2825		
		Examiner Name	Not yet assigned LIN, SUN J.		
Sheet	1	of	1	Attorney Docket Number	18021-6226

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JSR	A	R. Brayton et al., Logic Minimization Algorithms for VLSI Synthesis, Chapter 7, "Comparisons and Conclusions", pp. 160-173, 1984.	
JSR	B	J. Brzozowski et al., Asynchronous Circuits, Chapter 6, "Up-Bounded-Delay Race Models", pp. 83-111, 1994.	
JSR	C	J. Brzozowski et al., Asynchronous Circuits, Chapter 15, "Design of Asynchronous Circuits", pp. 314-367, 1994.	

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